AMENDMENTS TO THE CLAIMS:

The following listing of claims replaces all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device, comprising the steps of:

(a) forming a first insulating film including an organosiloxane as a main component over the first main surface of a semiconductor integrated circuit substrate;

(b) forming a patterned masking layer over said first insulating film; and

(c) subjecting said first insulating film, with said masking layer thereover, to plasma etching treatment in a gas atmosphere containing a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, in which atmosphere an argon gas as a carrier gas is the largest gas component, thereby forming a first recess in said first insulating film.

2. (Cancelled)

3. (Previously Presented) A manufacturing process of a semiconductor integrated circuit device according to claim 1, wherein said gas

atmosphere contains an oxygen gas.

4. (Previously Presented) A manufacturing process of a semiconductor integrated circuit device according to claim 1, wherein said gas atmosphere is substantially free of an oxygen gas.

5. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device, comprising the steps of:

(a) forming, over the first main surface of a semiconductor integrated circuit substrate, a first insulating film including an organosiloxane as a main component;

(b) forming, over said first insulating film, a second insulating film including as a main component a second organosiloxane which has a smaller carbon content than said first organosiloxane;

(c) forming a patterned masking layer over said second insulating film; and

(d) subjecting said second insulating film, while having said masking layer thereover, to plasma etching treatment with said first insulating film as an etching stopper, in a gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, thereby forming a first recess in said second insulating film.

6. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 5, wherein said second insulating film is thicker than said first insulating film.

7. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 6, wherein said first insulating film has a carbon content greater than said second insulating film by at least 50%.

8. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 6, wherein said first insulating film has a carbon content greater than said second insulating film by at least 100%.

9.-12. (Cancelled)

13. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device having an inlaid interconnect, comprising the steps of:

(a) forming, over the first main surface of a semiconductor integrated circuit substrate, a first insulating film constituting said inlaid interconnect;

(b) forming, over said first insulating film, a second insulating film which constitutes said inlaid interconnect and includes an organosiloxane as

a main component; and

(c) forming a patterned masking layer over said second insulating film;

(d) subjecting said second insulating film, with said masking layer thereover, to first plasma etching treatment in a first gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, thereby forming a first recess in said second insulating film; and

(e) subjecting said second insulating film, with said first recess formed therein, to second plasma etching treatment in a second gas atmosphere, containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, with said first insulating film as an etching stopper under the conditions wherein an etching selectivity to said second insulating film relative to said first insulating film is relatively large compared with that of said first plasma etching treatment, thereby exposing said first insulating film.

14. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 13, wherein upon completion of said step (d), the thickness of said second insulating film on the bottom surface of said recess is 30% or less of the initial thickness of said second insulating film.

15. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 13, wherein upon completion of said step (d), the thickness of said second insulating film on the bottom surface of said recess is 20% or less compared of the initial thickness of said second insulating film.

16. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 13, wherein upon completion of said step (d), the thickness of said second insulating film on the bottom surface of said recess is 15% or less of the initial thickness of said second insulating film.

17. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 14, wherein said first insulating film includes silicon nitride as a main component.

18.-21. (Cancelled)

22. (Withdrawn) A semiconductor integrated circuit device comprising:

(a) a first silicon nitride film, which is disposed over the first main surface of a semiconductor integrated circuit chip, is made of a silicon nitride or silicon oxynitride and has a first opening;

(b) a second insulating film which is disposed over said first silicon nitride film, includes a first organosiloxane having a smaller dielectric constant than said first silicon nitride film as a main component, and has a second opening connected with said first opening;

(c) a first interlevel dielectric film which is disposed over said second insulating film, includes an insulating film having a dielectric constant smaller than said first silicon nitride film as a main component, has a third opening which is connected with said second opening and constitutes, together with said first opening, a first through-hole, and a first interconnect-embedding trench connected with the third opening, and is thicker than said second insulating film;

(d) a first conductive barrier layer disposed to cover the bottom surface and inside surface of said first through-hole and the bottom surface and inside surface of said first interconnect-embedding trench; and

(e) a first interconnect region embedded in said first through-hole and said first interconnect-embedding trench, each having said first conductive barrier layer disposed therein and including copper as a main component.

23. (Withdrawn) A semiconductor integrated circuit device according to claim 22, wherein said second insulating film is thicker than said first silicon nitride film.

24. (Withdrawn) A semiconductor integrated circuit device according to claim 23, wherein said first interlevel dielectric film includes a second organosiloxane smaller in the number of carbon atoms than said first organosiloxane as a main component.

25. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device having an inlaid interconnect, comprising the steps of:

(a) forming, over the first main surface of a semiconductor integrated circuit substrate, a first insulating film constituting said inlaid interconnect;

(b) forming, over said first insulating film, a second insulating film including an organosiloxane as a main component and is for the formation of said inlaid interconnect;

(c) forming a patterned masking layer over said second insulating film; and

(d) subjecting said second insulating film, with said masking layer thereon, to first plasma etching treatment in a first gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, thereby forming a first recess in said second insulating film and exposing said first insulating film from said first recess.

26. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 25, wherein said first insulating film includes silicon nitride as a main component.

27. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 26, wherein said first gas atmosphere contains an argon gas as the largest gas component.

28. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 27, wherein said first gas atmosphere contains an oxygen gas.

29. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 27, wherein said first gas atmosphere is substantially free of an oxygen gas.

30. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device having an inlaid interconnect, comprising the steps of:

(a) forming, over the first main surface of a semiconductor integrated circuit substrate, a first insulating film which constitutes an interlevel dielectric film of said inlaid interconnect and includes a first organosiloxane as a main component;

(b) forming, over said first insulating film, a second insulating film which constitutes said inlaid interconnect, is thinner than said first insulating film and includes as a main component a second organosiloxane different in components from said first organosiloxane;

(c) forming a patterned masking layer over said second insulating film; and

(d) subjecting said second insulating film, while having said masking layer thereover, to first plasma etching treatment with said insulating film as an etching stopper in a first gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, thereby forming in said second insulating film a first recess and exposing therefrom said first insulating film.

31. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 30, wherein said second insulating film is thicker than said first insulating film.

32. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 31, wherein said first insulating film has a carbon content greater than said second insulating film by at least 50%.

33. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 31, wherein said first insulating film has a carbon content greater than said second insulating film by at least 100%.

34. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 31, wherein an etching selectivity to said second insulating film relative to said first insulating film in said step (d) is at least 4.

35. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 31, wherein an etching selectivity to said second insulating film relative to said first insulating film in said step (d) is at least 5.

36. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device having a dual-damascene type inlaid interconnect which is obtained by embedding a metal in a plug region for mutual connection between metallization layers and in an inlaid interconnect at the same time, comprising the steps of:

(a) forming, over the first main surface of a semiconductor integrated circuit substrate, a first insulating film constituting said inlaid interconnect;

(b) forming, over said first insulating film, a second insulating film which constitutes said inlaid interconnect and includes an organosiloxane as a main component;

(c) forming a patterned masking layer over said second insulating film;

(d) subjecting said second insulating film, with said masking layer formed thereover, to first plasma etching treatment in a first gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, thereby forming a first recess in said second insulating film; and

(e) subjecting said second insulating film, with said first recess formed therein, to second plasma etching treatment in a second gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, under the conditions wherein an etching selectivity to said second insulating film relative to said first insulating film is larger than that of said first plasma etching treatment, thereby exposing said first insulating film.

37. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 36, wherein said first insulating film includes silicon nitride as a main component.

38. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device having a dual-damascene type inlaid interconnect which is obtained by embedding a metal in a plug region for mutual connection between metallization layers and in an inlaid interconnect, comprising the steps of:

(a) forming, over the first main surface of a semiconductor integrated circuit substrate, a first insulating film for the formation of said inlaid interconnect;

(b) forming, over said first insulating film, a second insulating film, for the formation of said inlaid interconnect, which includes an organosiloxane as a main component;

(c) forming a patterned masking layer over said second insulating film; and

(d) subjecting said second insulating film, with said masking layer formed thereover, to first plasma etching treatment in a first gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen gas so as to avoid forming a sub-trench, by using said first insulating film as an etching stopper, thereby forming a first recess in said second insulating film and exposing said first insulating film from said recess.

39. (Original) A manufacturing process of a semiconductor integrated circuit device according to claim 38, wherein said first insulating film includes silicon nitride as a main component.

40. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device having a dual-damascene type inlaid interconnect which is obtained by simultaneously embedding a conductor film for the formation of both a plug region for mutual connection between metallization layers and an inlaid interconnect, comprising the steps of:

(a) forming, over the first main surface of a semiconductor integrated circuit substrate, a first insulating film which constitutes an interlevel dielectric film of said inlaid connect and includes a first organosiloxane as a main component;

(b) forming, over said first insulating film, a second insulating film which constitutes said inlaid interconnect, is thinner than said first insulating film and includes as a main component a second organosiloxane different in components from said first organosiloxane;

(c) forming a patterned masking layer over said second insulating film; and

(d) subjecting said second insulating film, while having said masking layer thereover, to first plasma etching treatment with said first insulating film as an etching stopper in a first gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a

nitrogen gas so as to avoid forming a sub-trench,~~,~~ thereby forming in said second insulating film a first recess and exposing therefrom said first insulating film.

41. (Currently Amended) A manufacturing process of a semiconductor integrated circuit device, comprising:

(a) forming an insulating layer including an organosiloxane homopolymer as a main component, over a main surface of a semiconductor substrate;

(b) forming a patterned masking layer over said insulating layer; and

(c) etching said insulating layer including said organosiloxane homopolymer with said patterned masking layer as a mask, said etching being performed by a plasma etching in a gas atmosphere containing an argon gas as a carrier gas, a fluorocarbon-gas-containing etching gas, and a nitrogen-containing gas so as to avoid forming a sub-trench.

42. (New) A manufacturing process of a semiconductor integrated circuit device according to claim 1, wherein said nitrogen gas is provided during the plasma etching treatment at a flow rate in a range of 50 sccm to 500 sccm.

43. (New) A manufacturing process of a semiconductor integrated circuit device according to claim 42, wherein the flow rate of the nitrogen gas is in a range of 150 sccm (C/N ratio: 0.16) to 300 sccm (C/N ratio: 0.08).